## SPECIFICATION AMENDMENTS

On page 4, first paragraph, please use the following substitute paragraph:

In [HP Docket Numbers 10013442 and 10013444], US Application Number 10/001,586 (Published Application Number 2003/0084249, and US Application Number 10/001,594 (Published Application Number 2003/0084253), filed concurrently with the present application, a single age-bit may be provided for each line in a cache, or for each index. Each time a line, or index, is accessed, or written, the corresponding age-bit is set to a first logical state. A state machine periodically checks the status of each age-bit. If an age-bit is in the first logical state, the state machine sets the age-bit to a second logical state. If the age-bit is already in the second logical state, then the line of data corresponding to the age-bit, or at least one line in the set of lines corresponding to the index corresponding to the age-bit, has not been accessed or changed since the last time the state machine checked the age-bit, and may be preemptively evicted.

On page 5, last paragraph, continuing on to page 6, please use the following substitute paragraph:

The following discussion provides one example of a cache memory system that includes timing to detect stale lines. The particular example is based on [HP Docket Numbers 10013442 and 10013444] US Application Number 10/001,586 (Published Application Number 2003/0084249, and US Application Number 10/001,594 (Published Application Number 2003/0084253), and is used for illustration only. However, the invention is applicable to any cache memory system that includes detection of stale lines based on time measurement.

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